REMARKS

The Office Action of 11/16/2007 has been carefully considered. Reconsideration in view of the foregoing amendments and the present remarks is respectfully requested.

Claim 10 has been allowed. Claims 3-9, 14 and 15 were indicated as containing allowable subject matter, which indication is appreciatively acknowledged.

Claim 11 has been amended to remedy the antecedent basis problem pointed out in the Office Action.

Claims 1,12 and 13 were rejected as being anticipated by Vicard. Claim 2 was rejected as being unpatentable over Vicard in view of Yamane. These rejections are respectfully traversed.

The present invention relates to a version-programmable circuit module that allows a single circuit module to be versioned to provide a range of performance levels. Such versioning may be achieved by providing a one-time-programmable (OTP) memory and programming the memory with a version number. An OTP memory, however, may require a different fabrication process than a circuit whose performance is to be versioned, thereby entailing costly modifications. To address this problem in a cost-effective way, the invention provides for a module having first and second sub-circuits, the first sub-circuit being the circuit whose performance is to be versioned. The first sub-circuit includes a version number memory. However, this memory need not be an OTP memory but rather can be a memory fabricated using the same process as the functional

circuitry of the first sub-circuit. A second sub-circuit is provided having a write-protected memory (such as an OTP memory). The first and second sub-circuits are coupled by a communication link. A version number control circuit sends update values for the version number memory from the write-protected memory via the communication link. The invention is not intended to provide upgradeability.

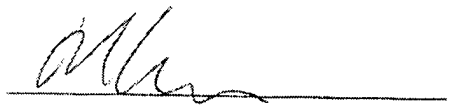
The rejection is flawed for various reasons, the most obvious being that the rejection identifies the register 25 (Fig. 1 of Vicard) as ***both*** the claimed version number memory and the claimed write-protected memory. Such identification makes no sense in the context of the claims. Claim 1, for example, claims a version number control circuit arranged to send update values for the version number memory from the write-protected memory via a communication connection. There is no updating of the register 25 in Vicard, which is written permanently a single time. Nor would it make any sense for the register 25 to update itself. Nor would it make sense to provide a communication connection for the register 25 to update itself.

In relation to the foregoing feature of claim 1, the rejection cites Vicard sending enable signals from comparison block 27 to functional blocks 12A-12E depending on the signature sent from the register 25 to the comparison block 27 (Figs. 1 and 2, col. 7, lines 34-59, col. 8, lines 1-14 of Vicard). Such enable signals have no effect on the register 25 and cannot be said to be "update values for the version number memory."

In dependent claim 12 is believed to be allowable for similar reasons.

Withdrawal of the rejections and allowance of claims 1-15 is respectfully requested.

Respectfully submitted,



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